Atty. Docket No. PIA31223/DBE/US
Serial No: 10/751,212

Remarks

Applicant and his representatives wish to thank Examiner Ha for the thorough examination of the present application, and the detailed explanations in the Office Action dated December 20, 2005. Applicant has carefully reviewed the Examiner's Office Action, and respectfully traverses the new grounds of rejection below.

The present invention relates to a method for packaging a semiconductor device, including the steps of (a) forming an Au bump on a bond pad of a wafer, (b) dicing the wafer into a chip, and (c) attaching the Au bump of the chip to a substrate to form a flip-chip bond by using a thermo-pressure process. Although the Office Action appears to assert that the metal balls 80 of Soga et al. (U.S. Pat. Appl. Publ. No. 2002/0171157) correspond to the Au bump of the present claims, the art appears to recognize differences between the metal balls 80 of Soga et al. and the Au bump of the present claims. The present invention is thereby believed to enable miniaturization of the semiconductor device, simplification of the packaging process, and reduced costs, relative to the method of Soga et al.

The references cited by the Examiner (Soga et al. and Fukao et al. [U.S. Pat. Appl. Publ. No. 2003/0011078]) neither disclose nor suggest attaching an Au bump on the bond pad of a wafer to a substrate. Thus, the present claims are patentable over the cited references.

The Rejection of Claims 1-3 under 35 U.S.C. § 102(a)

The rejection of Claims 1-3 under 35 U.S.C. § 102(a) as being anticipated by Soga et al. is respectfully traversed.

Soga et al. disclose junctions formed between a semiconductor device and a substrate, comprising metal balls (Cu, etc.) and compounds of Sn and the metal balls, and the metal balls are bonded together by the compounds (Abstract). With regard to FIGS. 16(a)-(d), Soga et al. disclose a package of a chip 25 and junction substrate 14, obtained by the temperature-hierarchical bonding of Pb-free solder by use of Cu balls 80 (Soga et al., p. 12, paragraph [0115]). As regards the shape of a bump, Soga et al. disclose a ball bump (FIG. 16(b)), a wire

bond bump (FIG. 16(c)) and a Cu-plated bump of a readily deformable structure (FIG. 16(d)) (Soga et al., p. 12, paragraph [0115]).

Although Soga et al. use the term "bump" to describe Cu balls 80, it is believed that this term merely refers to a deformed shape of Cu balls 80. For example, Soga et al. teach that in the case shown in FIG. 16(a), Soga et al. form bonds by feeding Sn onto a thin-film pads 82 on the side of the Si chip 25 by vapor deposition, plating, a paste, or the composite paste including metal balls and solder balls; thermally pressure-bonding thereto metal balls 80 such as balls of Cu, Ag, Au, etc. or Au-plated Al balls, or metallized organic resin balls to thereby form an intermetallic compound 84 with Sn; then bonding to a junction substrate (Soga et al., p. 12, paragraph [0115]). This disclosure is consistent with the understanding in the art that solder balls or metal balls are typically used in flip chip bonding (see, e.g., Wolf, Silicon Processing for the VLSI Era, Volume 1 – Process Technology [2nd ed. 2000], p. 858, last 5 lines; previously submitted with the Amendment filed October 12, 2005), whereas Au bumps (as that term is generally understood in the art) appears to be associated with tape automated bonding (or TAB; see Wolf, p. 854, ll. 2-5 from the bottom, and p. 855, submitted herewith). Consistent with the understanding in the art, the Au bump of the present Claim 1 may have a pillar shape (see, e.g., Au bump 200 in FIG. 3A of the present application). Thus, it is believed that the alternative Au, etc. or Au-plated Al balls that may form the ball bump or wire bond bump of Soga et al (FIGS. 16(b)-(c)) are different from, and not equivalent to, the Au bump recited in Claim 1 (further compare, e.g., the paragraph bridging pp. 1-2 of the present specification with p. 2, ll. 9-21 of the present specification).

Further, since the metal balls 80 of Soga et al. are ball-shaped, the metal balls 80 are believed to have a relatively small contact surface with the chip 25, and it is believed that they cannot be readily attached to the chip 25 and that they show low interconnectivity. Therefore, it is believed that the metal balls 80 cannot be directly connected to the chip 25, and additionally require the processes of forming thin film pad 82 and intermetallic compound 84 to connect the metal balls 80 to the chip 25. In contrast, the Au bump of the present Claims 1-3 can be pillar-shaped, as stated above. As a result, the presently claimed Au bump can be directly connected to

the chip (e.g., through an interface metallurgy on a bond pad, as disclosed by Wolf in Fig. 17-11, p. 856, submitted herewith), without using both the intermetallic compound 84 **and** the thin film pad 82 as disclosed by Soga et al.

Soga et al. also discloses a flip chip mounting structure in FIG. 5(a), in which Si chips 8 are bonded by die bonding while the terminals are connected by wire bonding (see, e.g., Soga et al., page 8, paragraph [0086]). Although Soga et al. discloses Au or Cu bumps 18 of each of the Si chips bonded to the junction substrate 35 by supplying a paste thereto (see, e.g., Soga et al., page 8, paragraph [0086]), the Au or Cu bumps 18 of FIG. 5(a) appear to be metal balls, as disclosed in the Abstract, shown in FIG. 16(a), and as described later in paragraph [0086] (i.e., "where Au ***ball*** bumps are used while Sn-plated terminals are provided on the substrate"; see Soga et al., page 8, paragraph [0086], ll. 26-30; emphasis added).

As Applicant stated earlier in prosecution, a typical flip chip bonding process does not include the steps of forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate using a thermo-pressure process. A typical flip chip bonding process includes the steps of forming balls on the bond pads, flipping the chip over to place the balls in contact with the substrate, and applying a reflow process to attach the solder balls to the substrate (see, e.g., Wolf, pp. 857-858, previously submitted.) The disclosure of Soga et al. appears to be consistent with this understanding and with Applicant's positions. Therefore, Soga et al. do not disclose or suggest forming an Au bump on a bond pad and attaching the Au bump of the chip to a substrate, as recited in Claim 1.

Consequently, this ground of rejection is believed to be unsustainable, and Applicant respectfully requests withdrawal thereof.

The Rejection of Claim 4 under 35 U.S.C. § 103(a)

The rejection of Claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Soga et al. and Fukao et al. is respectfully traversed.

As discussed above, Soga et al. is believed to be deficient with regard to attaching an Au bump as recited in the present Claim 1. Fukao et al. fails to cure this deficiency.

The disclosure of Fukao et al. relates to a semiconductor module and producing method therefor (Title). Fukao et al. disclose that a gold bump or a nickel bump 7 is applied to the pad portion 2a of a bare IC chip 2 (see Fukao et al., p. 4, paragraph [0079]). However, Fukao et al. directly connect an end of a lead terminal 3 to the pad portion 2a of the bare IC chip 2 to via a bump 7 made of gold, nickel, solder or the like (see Fukao et al., p. 4, paragraph [0080], and FIG. 2). Therefore, it is believed that Fukao et al. do not disclose or suggest attaching the Au bump of the chip to a substrate to form a flip-chip bond.

As a result, it is believed that neither Soga et al. nor Fukao et al. disclose attaching an Au bump on a bond pad of a chip to a substrate to form a flip chip bond. Therefore, it is believed that no combination of the two references can disclose or suggest all of the limitations of Claim 1, and Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. § 103(a) of Claim 4 (which depends from Claim 1).

Conclusions

In view of the above remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

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If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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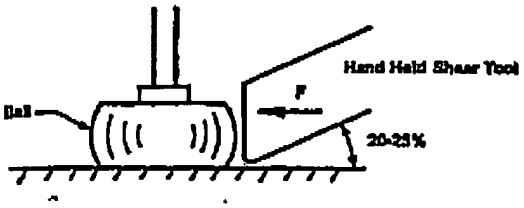

Fig. 17-8 Ball shear test setup, showing the manual shear probe in use.[22]

a gold (Au) bump (in TAB), or a solder ball (in flip-chip) is placed over the pad. This protects the corrosion sensitive Al. ICs assembled with the latter methods can exhibit reduced device failure rates from corrosion over devices assembled with wire bonding.

17.5.2 Wire Bond Spacing

As the number of external connections to an IC increases, a larger number of bond pads on the chip are needed. Since the number of such pads is increasing faster than the chip size, the bond pad *pitch* (bond pad center-to-center distance) must decrease, especially if the bond pads are along the periphery of the chip (as is the case with wire bonds). In memory chips, the pads are located along only two facing sides of the chip (or in the chip center for LOC packages, see Sect. 17.10.1). In logic and microprocessor chips the I/O count is increasing and the active device size is decreasing. Thus, the interconnect area represents a large fraction of the total Si area. In some cases, it may even determine the chip size, as extra space is needed around the active area for additional pad placement. The minimum wire bonding pitch has been steadily declining, and by 1998 had decreased to 50–80 μm (with 23 μm wires). The wire span from the chip to the package is typically 1 to 4 mm. Longer wires could lead to shorts to adjacent wires, as longer wires are more likely to droop or deform. In plastic packages, longer wires can also deform due to resin flow during the molding operation. To allow more wire bonds to be made on a chip, while meeting the minimum pad pitch and wire length requirements, staggered bond pads and package terracing are sometimes employed as a solution (Fig. 17-9).

17.5.3 Tape Automated Bonding (TAB)

For chips that require high pin counts (e.g., more than about 208 pins), wire bonding becomes undesirable, as the chip size must grow to accommodate the space for the wire-bond pads. An alternative chip-pad to package-pad connection method called *tape-automated bonding* (TAB) has been developed to handle such applications. In the TAB method, the wires of wire-bonding are replaced with finely patterned thin metal leads (usually made of Cu foil, plated with Au or Sn). The TAB method involves bonding silicon chips to patterned metal-on-polymer tape by thermocompression bonding (prior to the die-attach procedure). Usually, these leads are formed by depositing the metal film onto a flexible strip of polymer tape. Then this film is patterned by lithographic techniques similar to those used in the IC fabrication process. This forms the desired lead pattern, and the result is a strip of tape containing many individual lead systems (Fig. 17-10). The most popular way of connecting these leads to the chip involves the creation of bumps on the chip bonding pads (formed by electroplating Au). The tape is moved by sprockets until one of the lead systems is positioned exactly over the chip and the leads are then thermally bonded to these bumps. Note, however, that variations to the TAB process described above have also been used commercially (see Ref. 12).

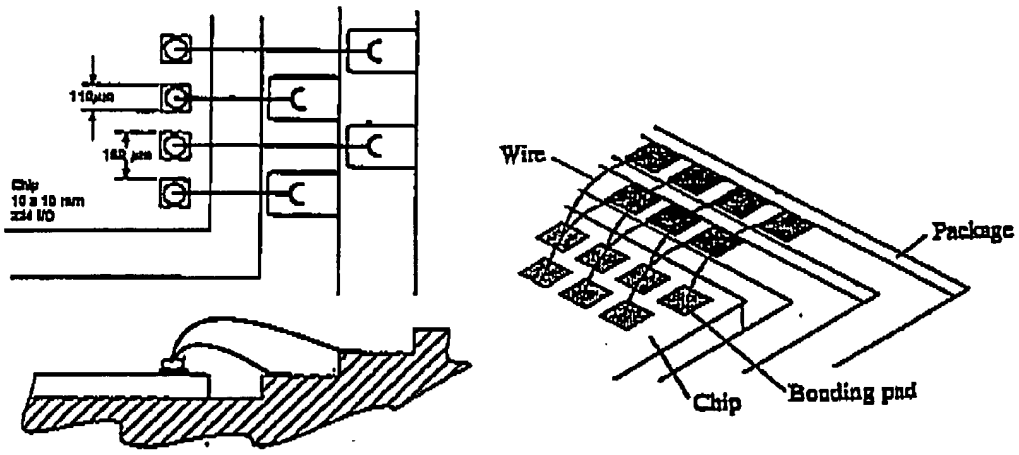

Fig. 17-9 Bond pads staggered on different levels. Chip and bonding pad configuration.[11] © ISHM.

The fabrication of the bumps on the bond pads is a multi-step process (Fig. 17-11). First a multi-layer metal film (consisting of Cr, Cu, and Au layers) is sputter-deposited in blanket form onto the wafer surface (which is covered with a passivation oxide layer, except for the bond pad. Lithography is then used to create patterns in a photoresist film that will act as a 25–30 μm-thick mask for the Au electroplating step. That is, openings in the resist are created over the bonding pads, where electroplating is then used to deposit Au bumps, 10-30 μm thick. Next, the resist is stripped. Finally, to complete the bump formation, the diffusion-barrier film is etched.

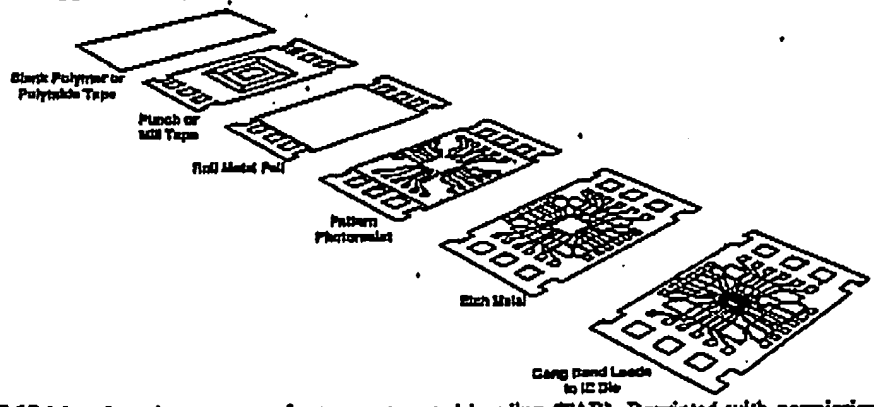

Fig. 17-10 Manufacturing sequence for tape-automated bonding (TAB). Reprinted with permission of Integrated Circuit Engineering Corporation.

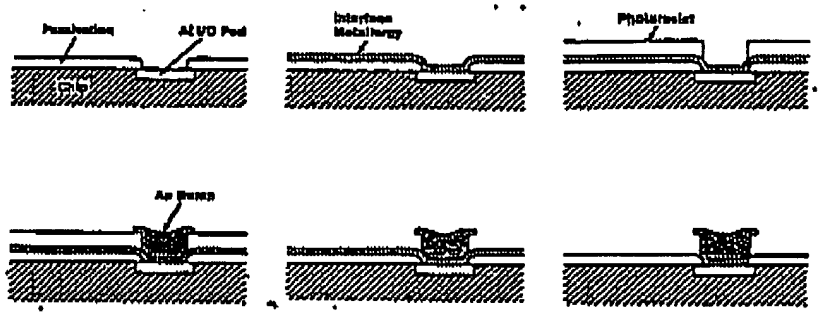

Fig. 17-11 Gold bump processing for TAB.[13] Reprinted with permission of Solid State Technology.

The Au bumps protect regions of the barrier layer film underneath them from being etched during this step.

The bonding of the metal leads to the bumps on the chip is done simultaneously by thermocompression (Fig. 17-12). That is, a heated *thermode* (300–360°C) is pressed against the leads, which are each pressing against a bump on the chip. The heated thermode applies a load of about 10 kg/mm^2 for 1–2 seconds to form the bond between the lead and bump. This step is known as *inner-lead bonding*. At this point, the chip has been attached to the tape that carries the lead pattern. Next, the chip and lead pattern are encapsulated (while they are still attached to the strip of tape), usually by plastic molding (Fig. 17-13). The packaged chips are separated from the continuous tape that carries the leads, to form an individual packaged part. These packaged parts are finally attached to a *printed wiring board* (*PWB*) by a process called *outer-lead bonding* (Fig. 17-14). That is, the packaged chip with the leads in place is transferred to the PWB, where the leads are attached to the land patterns on the board (usually by a lower temperature bonding process, such as *pulse-thermode reflow*, to protect the PWB laminate).

In addition to allowing bonding pads with smaller pitches than the ones needed for wire bonding, TAB offers the advantages of speed (since all the bonds are formed at once), and the ease of automation offered by the tape and sprocket system. Since the leads have no loop (as do

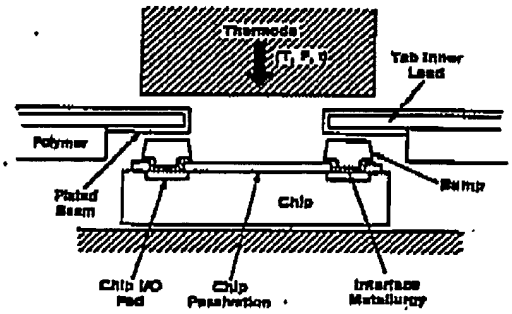

Fig. 17-12 TAB inner lead bonding.[2] Reprinted with permission of Van Nostrand Reinhold.